Claims

[c1] 1.A bus-switch chip protected from pin-to-pin electro-static-discharge (ESD) pulses comprising:

a first pin;

a second pin;

a bus-switch transistor having a drain coupled to the first pin and a source coupled to the second pin and a gate coupled to a bus-switch gate node, the bus-switch transistor connecting the first pin to the second pin when an activating voltage is applied to the bus-switch gate node, but isolating the first pin from the second pin when an isolating voltage is applied to the bus-switch gate node during normal operation when power is applied to the bus-switch chip;

a first coupling capacitor, coupled between the first pin and a first coupling-gate node, for generating an activating voltage on the first coupling-gate node during an ESD pulse applied to the first pin;

a first coupling transistor responsive to the first coupling-gate node, for connecting the first pin to a first grounding-gate node when the first coupling capacitor generates the activating voltage on the first-coupling gate node; and

a first grounding transistor, responsive to the first grounding-gate node, for connecting the second pin to the bus-switch gate node when the first coupling transistor connects the ESD pulse on the first pin to the first grounding-gate node,

whereby the bus-switch transistor is shut off by being connected to the second pin when the ESD pulse is applied to the first pin.

[c2] 2.The bus-switch chip of claim 1 wherein the bus-switch transistor, the first coupling transistor, and the first grounding transistor are n-channel transistors.

[c3] 3.The bus-switch chip of claim 2 wherein the activating voltage is a voltage at least a transistor-threshold above a source voltage.

[c4] 4.The bus-switch chip of claim 1 further comprising a reverse-isolation circuit that comprises:

a second coupling capacitor, coupled between the second pin and a second

coupling-gate node, for generating an activating voltage on the second coupling-gate node during an ESD pulse applied to the second pin;

a second coupling transistor responsive to the second coupling-gate node, for connecting the second pin to a second grounding-gate node when the second coupling capacitor generates the activating voltage on the second-coupling gate node; and

a second grounding transistor, responsive to the second grounding-gate node, for connecting the first pin to the bus-switch gate node when the second coupling transistor connects the ESD pulse on the second pin to the second grounding-gate node,

whereby the bus-switch transistor is shut off by being connected to the first pin when the ESD pulse is applied to the second pin.

[c5] 5.The bus-switch chip of claim 4 wherein the first coupling transistor is larger than the first grounding transistor.

[c6] 6.The bus-switch chip of claim 5 wherein the first coupling transistor is larger than the second grounding transistor.

[c7] 7.The bus-switch chip of claim 5 wherein the first coupling transistor is at least twice as large as the first grounding transistor.

[c8] 8.The bus-switch chip of claim 4 further comprising:

a first protection device, connected between the first pin and an internal ground bus, for shunting current from the ESD pulse applied to the first pin to the internal ground bus;

a second protection device, connected between the second pin and the internal ground bus, for shunting current from the ESD pulse applied to the second pin to the internal ground bus.

[c9] 9.The bus-switch chip of claim 8 wherein the second pin is grounded and the internal ground bus is floating when the ESD pulse is applied to the first pin during a pin-to-pin ESD test;

wherein the ESD pulse is dissipated by shunting current from the first pin through the first protection device to the internal ground bus, and from the

internal ground bus to the second pin through the second protection device.

[c10] 10.The bus-switch chip of claim 8 further comprising:
a first leaker device for discharging the first grounding-gate node after the ESD pulse is applied to the first pin to turn off the first grounding transistor after the ESD pulse on the first pin has ended;
a second leaker device for discharging the second grounding-gate node after the ESD pulse is applied to the second pin to turn off the second grounding transistor after the ESD pulse on the second pin has ended,
whereby the first and second grounding-gate transistor are turned off after ESD pulses end.

[c11] 11.The bus-switch chip of claim 10 further comprising:
a third leaker device for discharging the first coupling-gate node after the ESD pulse is applied to the first pin to turn off the first coupling transistor after the ESD pulse on the first pin has ended;
a fourth leaker device for discharging the second coupling-gate node after the ESD pulse is applied to the second pin to turn off the second coupling transistor after the ESD pulse on the second pin has ended.

[c12] 12.The bus-switch chip of claim 11 wherein the first, second, third, and fourth leaker devices are resistors to the internal ground bus or are n-channel transistors each having a gate coupled to an internal power supply and a source coupled to the internal ground bus.

[c13] 13.A shock-protected integrated circuit comprising:
a first input that can receive an electric shock pulse;
a second input that can be grounded when the electric shock pulse is applied to the first input;
switch transistor means for conducting current between the first input and the second input in response to an enabling voltage applied to a control node, but for isolating the first input from the second input when an isolating voltage is applied to the control node;
first capacitor means for capacitivly coupling an enabling voltage to a first node when the electric shock pulse is applied to the first input;

first coupling transistor means for conducting current from the first input to a first gate node in response to the enabling voltage on the first node; and

first disabling transistor means, responsive to the first node, for conducting current between the control node and the second input to generate the isolating voltage on the control node to disable the switch transistor means when the first coupling transistor means conducts the electric shock pulse to the first node,

whereby the electric shock pulse causes the switch transistor means to isolate the first input from the second input.

[c14] 14.The shock-protected integrated circuit of claim 13 further comprising:

first protection means for protecting the switch transistor means from the electric shock pulse applied to the first input by shunting current to an internal supply bus;

second protection means for protecting the switch transistor means from an electric shock pulse applied to the second input by shunting current to the internal supply bus.

[c15] 15.The shock-protected integrated circuit of claim 14 wherein the internal supply bus is floating when the electric shock pulse is applied to the first input, whereby shock protection is provided when the internal supply bus is floating.

[c16] 16.The shock-protected integrated circuit of claim 15 wherein the second input receives a second electric shock pulse and the first input is grounded during a reverse shock condition;

further comprising:

second capacitor means for capacitivly coupling an enabling voltage to a second node when the second electric shock pulse is applied to the second input;

second coupling transistor means for conducting current from the second input to a second gate node in response to the enabling voltage on the second node; and

second disabling transistor means, responsive to the second node, for conducting current between the control node and the first input to generate the isolating voltage on the control node to disable the switch transistor means

when the second coupling transistor means conducts the second electric shock pulse to the second node,

whereby the second electric shock pulse causes the switch transistor means to isolate the second input from the first input.

[c17] 17.The shock-protected integrated circuit of claim 16 wherein the switch transistor means comprises an n-channel transistor.

[c18] 18.An electro-static-discharge (ESD) isolation circuit comprising:

a bus-switch transistor having a drain connected to a first pad, a source connected to a second pad, and a gate connected to a bus-switch gate node;

a first capacitor coupled between the first pad and a first control-gate node;

a first coupling transistor having a gate connected to the first control-gate node, a drain connected to the first pad, and a source connected to a first isolating-gate node;

a first isolating transistor having a gate connected to the first isolating-gate node, a source connected to the second pad, and a drain connected to the bus-switch gate node;

a second capacitor coupled between the second pad and a second control-gate node;

a second coupling transistor having a gate connected to the second control-gate node, a drain connected to the second pad, and a source connected to a second isolating-gate node;

a second isolating transistor having a gate connected to the second isolating-gate node, a source connected to the first pad, and a drain connected to the bus-switch gate node.

[c19] 19.The ESD isolation circuit of claim 18 further comprising:

a first ESD-protection device connected to the first pad and to an internal bus;

a second ESD-protection device connected to the second pad and to the internal bus.

[c20] 20.The ESD isolation circuit of claim 19 wherein the first and second coupling transistors, the first and second isolating transistors, and the bus-switch transistor are n-channel transistors.